Chapter-1

2 marks question :-

Q . Define knee voltage .[2014]

The forward voltage at which the current through the pn junction starts increasing rapidly is called as cut in voltage or knee voltage.

It is approximately equal to the barrier potential of the diode .

Q . What is avalanche breakdown ?[2015]

Avalanche breakdown is a phenomenon that can occur in both insulating and semiconductor materials.It is a form of electric current multiplication that can allow very large currents within materials which are otherwise good insulators.It is a type of electron avalanche.

5 markes questions :-

Q . Explain the difference between zener breakdown and avalanche breakdown [2014].

Zener breakdown :-	**Avalanche breakdown :-**
1.Both sides of pn junction are heavily doped.	1.Both sides of pn junction are Lightly doped.
2.Depletion layer is narrow.	2.depletion layer is large.
3.A strong electric field is produced.	3.Electric field is not so strong.
4,Large number of holes and electrons are produced	4.Electron hole pair is generated .
5.Zener current is independent of applied energy from the applied potential.	5.Charge carriers acquire Voltage .

7 markes questions:

Q. <u>What is a pn junction ?explain the vi characteristics of pn junction diode under forward and reverse biasing with a neat diagram.</u>

When a pn type semiconductor is suitably joinedto ntype semiconductor ,the contact surface is called pn junction.

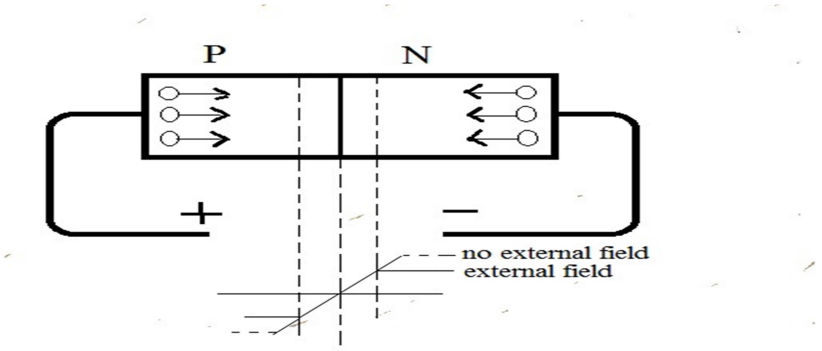
In actual practice ,the characteristic properics of pn junction will not be apparent .if a p type block is just brought in contact with n type block.

It is fabricated by special techniques and one common method of making pn junction is called alloying .

Pn junction under forward biasing

When external dc voltage applied to the junction is in such a direction that it cancels the potential barrier thus permitting current flow ,is called forward biasing.

To apply forward bias ,connect +ve terminal of the battery to ptype and –ve terminal to n type.

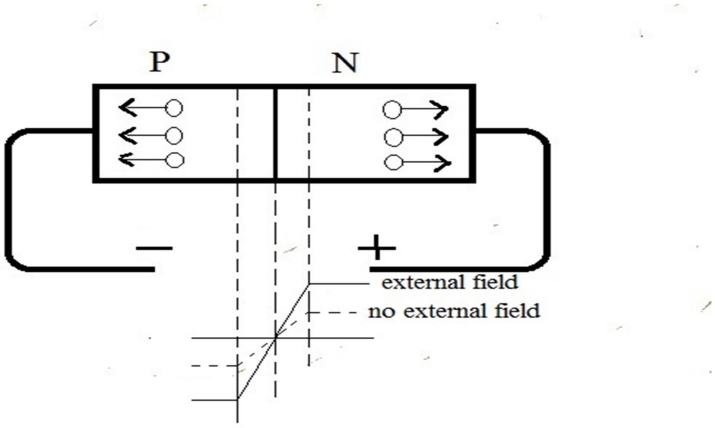


The applied forward potential establishes an electric field which acts against the field due to potential barrier.therefore ,the resultant field is weakened and the barrier height is reduced at the junction .

Pn junction under reverse biasing

When the external dc voltage applied to the juncton is in such a direction that potential barrier is increased ,it is called reverse biasing .

To apply reverse bias ,connect –ve terminal of the battery to p type and +ve terminal to n type.



The increased potential barriers prevents the flow of charge carriers across the junction .

Q . <u>Describe the operation of clipping and clamping circuit with proper diagram.[2015]</u>

clipping

The circuit with which the waveform is shaped by removing a portion of the applied wave is known as a clipping circuit.

Clippers find extensive use in rader ,digital and other electronic system.

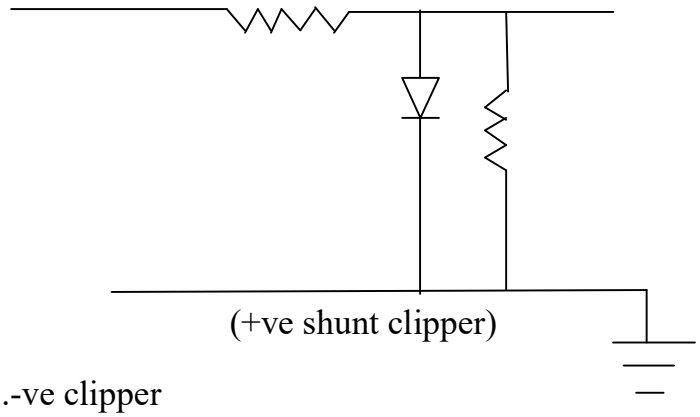
The important diode clppers are

1.+ve clipper

It is of 2 types

A)+ve series

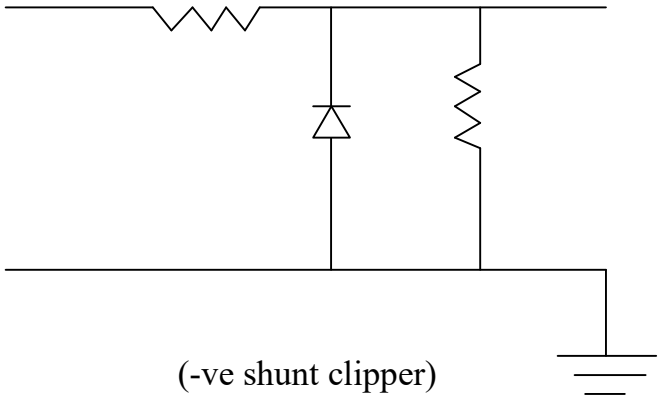
B)+ve shunt



2.-ve clipper

a)-ve series

b)-ve shunt



(-ve shunt clipper)

When both +ve and –ve half cycle of the input voltage is to be clipped.

Clamping

A climping circuit is used to place either the +ve or –ve peak of a signal at a desired level .The dc component is simply added or substracted from the input signal .It is also two types 1)+ve clamper and 2)-ve clamper

Chapter 2

2 marks questions

Q.What are thermistors ?[2014]

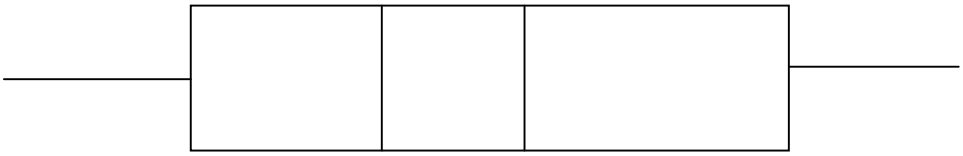
Thermistors are one of the mot commonly used devices for the measurement of temperature.The thermistors are resistors whose resistance changes with the temperature ,while for most of the metals, the resistance increases with temperature ,the thermistors respond negatively to the temperature and their resistance decreases with the increase in temperature .Since the resistance of thermisors is dependent on the temperature ,they ca be connected in the electrical circuit t measure the temperature of the body.

Q.what will happen if a zener diode is used in forwad biased condition [2015] .

Zener diodes are made in such a way that they resist some limited voltage in reverse bias,but in forward biased condition .the diodeworks simply like any other PN junction diode .

5 marks questions

Q.PIN diode[2015]



A pin diode is a diode with a wide ,undoped intrinsic semiconductor region between a p type semiconductor and an n type semiconductor region.The p type and n type regions are typically heavily doped because they are used for ohmic contacts.

Operation :

A pin diode operates under what is known as high level injection .In other words ,the intrinsic “i” region is flooded with charge carriers from the “p” and “n” regions .Its function the can be likened tofilling up a water bucket with a hole on the side.Oncethe water reaches the hole’s level it will begin to pour out.

Similarly ,the diode will conduct current once the flooded electrons and holes reach an equilibrium point ,where th number of electrons is equal to the number of holes in the intrinsic region .

Characteristics :

A pin diode obeys the standard diode equation for low frequency signals .At higher frequencies ,the diode looks like an almost perfect resistor.

Chapter 3

2 makes questions

Q.Define transformer utilization factor [2014] .

Transformer utilization factor (TUF) of a rectifier circuit is defined as the ratio o the dc power available at he load resistor and the ac rating of the secondary coil of a transformer.It can be used to determine the VA rating of a transformer .Actualy it is measure of merit of a rectifier circit .

$$TUF = V_{dc}I_{dc} / V_sI_s$$

Rms values

Q.Define ripple factor[2015].

Ripple factor may be defined as the ratio of the root mean square (rms) value of the ripple voltage to the absolute value of the dc component of the output voltage ,usually expressed as a percentage .Hoeever ,ripple voltage is also commonly expressed as the peak o peak value.

Q.What is filter and need of filter [2015] .

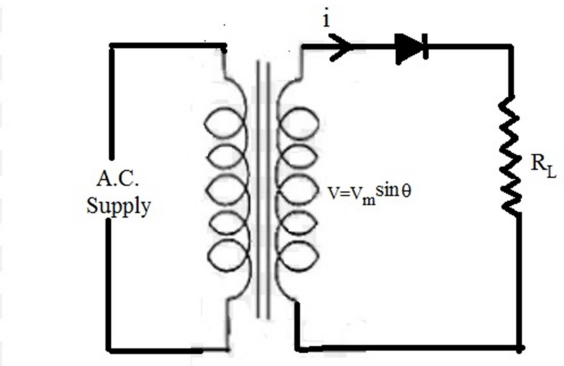
A filter circuit is a device which removes the a.c. component of rectifier output but allows the d.c. component to reach the load.It is of different types ,they are capacitor ,filter ,choke input filter and capacitor input filter or π filter .

5 markes questions

Q.Derive an expression for the efficiency of a half wave rectifier[2014]

The ratio of d.c. power output to the applied input a.c. power is known as rectifier efficiency i.e ,

Rectifier efficiency ,$=\frac{output\ d.c.power}{input\ a.c.power}$



Concider a half wave rectifier shown above .let $V=V_m \sin\Theta$ be the alternating voltage that appears across the secondary winding .let r_f and R_l be the diode resistance and load resistance respectively .the diode conducts during positive half cycles of a.c supply while no current condition takes place during negative half cycles .

d.c power :

The output current is pulsating direct current .Therefore ,in order to find d.c. power average current has to found out .

$$I_{av} = I_{dc}\frac{1}{2\pi}\int_0^{\pi} id\theta$$

$$= \frac{1}{2\pi}\int_0^{\pi}\frac{V_m \sin\theta}{r_f + R_L}d\theta$$

$$= \frac{V_m}{2\pi(r_f + R_L)}\int_0^{\pi} sin\theta\, d\theta = \frac{V_m}{2\pi(r_f + R_L)}[-cos]_0^{\pi} = \frac{V_m}{2\pi\left(r_f + R_L\right)} \times 2$$

$$= \frac{V_m}{r_f + R_L} \times \frac{1}{\pi} = \frac{I_m}{\pi} \qquad [\because I_m$$

$$= \frac{V_m}{r_f + R_L}]$$

$\therefore$ d.c. power ,$I_{dc}^2 \times R_L = (\frac{I_m}{\pi}) \times R_L$ ———————— (1)

a.c. power input :the a.c. power input is given by $p_{ac} = I_{rms}^2(r_f + R_L)$

for a half wave rectified wave ,$I_{rms} = \frac{I_m}{2}$

$P_{ac} = (\frac{I_m}{2})^2 \times \left(r_f + R_L\right)$ ———————— (2)

Rectifier efficiency $= \frac{d.c\ output\ power}{a.c.input\ power} = \frac{(I_m/\pi)^2 \times R_L}{(I_{m/2})^2(r_f + R_L)}$

$\therefore$ max $rectifier\ efficiency = 40.6\%$

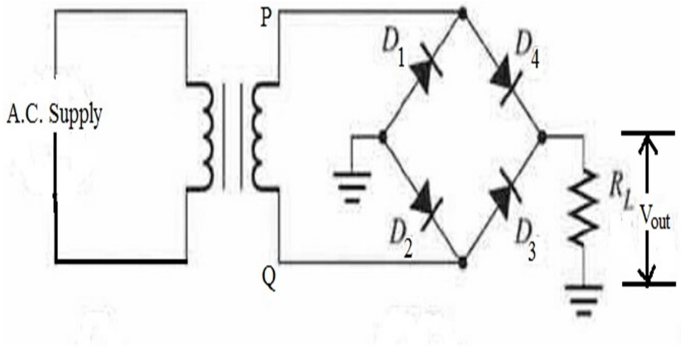
7 marks questons

Q.<u>Explain the working of a full wave bridge rectifier with suitable circuit diagram and wave forms .what is the efficiency and ripple factor of a full wave rectiier .[2014]</u>

Full wave bridge rectifier :

The need for a center tappd power transformr is eliminated in the bridge rectifier .it contains 4 diodes D_1 ,D_2 ,D_3 and D_4 connected to form bridge .

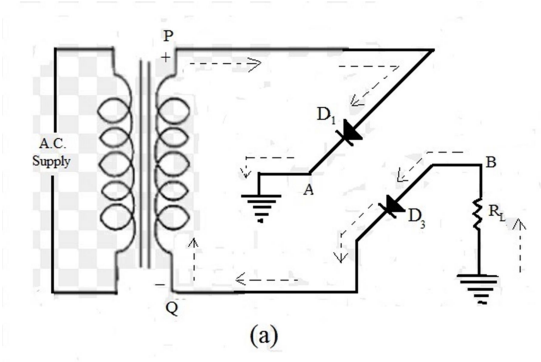
The a.c supply to be rectified is applied to the diagonally opposite ends of the bridge through the transformer between other two ends of the bridge ,the load resistance R_L is connected .

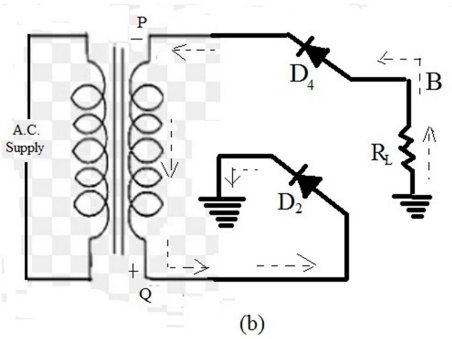


Operation :-

During the +ve half cycle of secondary voltage the end P of the secondary winding becomes +ve and end Q –ve .This makes diodes D_1 and D_3 forward biased while ,diodes D_2 and D_4 are reverse biased ,Therefore ,only diodes D_1 and D_3 conduct .These two diodes will be in series through yhe load R_L as shown in figure (a) .The conventional current flow is shown by dotted arrows .It may be seen that current flows from A to B through the load R_L .

During the –ve half cycle of secondary voltage ,end P becomes –ve and end Q posiive .This makes diodes D_2 and D_4forward biased where as diodes D_1 and D_3 are reverse biased .Therefore ,only diodes D_2 and D_4 conduct .These two diodes will be I series through the load R_L as shown in fig (b) .The current flow is shown by the solid arrows .It may be seen that again current flows from A to B through the load i.e in the same direction as for the positive half cycle .Therefore d.c. output is obtained across load R_L .





Efficiency of full wave rectifier :

Full waave rectification efficiency is $= \frac{d.c.\ output\ power}{a.c.\ input\ power}$

$$= \frac{P_{d.c.}}{P_{a.c.}} = \frac{(\frac{2I_m}{\pi})^2 R_L}{(\frac{I_m}{\sqrt{2}})^2 (r_f + R_L)}$$

$$= \frac{8}{\pi^2} \times \frac{R_L}{(r_f + R_L)} = \frac{0.812 R_L}{r_f + R_L}$$

$$= \frac{0.812}{1 + \frac{r_f}{R_L}}$$

Ripple factor of full wave rectifier :

The ratio of r.m.s value of a.c. component to the d.c. component in the rectifier output is known as ripple factor.

Ripple factor for full wave rectification

$$I_{r.m.s} = \frac{I_m}{\sqrt{2}} \quad , \quad I_{d.c} = \frac{2I_m}{\pi}$$

Ripple factor $= \sqrt{(\frac{I_m/\sqrt{2}}{2I_m/\pi})^2} - 1 = 0.48$

Chapter 4

5marks questions

Q.Explain about the current components in a transistor .[2014]

1.current conduction in NPN transistor is because of electrons and that in PNP is due to holes .The conventional flow of current is in the opposite direction .

2.The current flowing through the emitter is called as the emitter current (IE) ,this emitter current is composed of 2 components one because of holes and other because of electrons .

3.Since the emitter is heavily doped and the base is lightly doped thus the emitter current because of electrons is so very small as compared to the hole current .

4.All the holes crossing the emitter junction do not reach the collector as some of the recombine in the base region .

5.Ihc is the hole current in the collector region ,now some electrons recombine in the base region so this current Ihc is smaller than the IhE .

6.When emitter is closed then IC=IhC+ICo

7.In the active mode of operation the collector current is given as

IC=αIE+ICo ,where α is the large signal current gain .

Q.<u>Derive relation between α ,β and γ [2015] .</u>

$$\Delta I_E = \Delta I_B + \Delta I_C$$

1)Relation between α and β :-

As , $\beta = \frac{\Delta I_c}{\Delta I_B} = \frac{\Delta I_C}{\Delta I_E - \Delta I_C} = \frac{\Delta I_C/\Delta I_E}{1-\Delta I_C/\Delta I_E} = \frac{\alpha}{1-\alpha}$

As , $\alpha = \frac{\Delta I_C}{\Delta I_E} = \frac{\Delta I_C}{\Delta I_B + \Delta I_C} = \frac{\Delta I_C/\Delta I_E}{1+\Delta I_C/\Delta I_B} = \frac{\beta}{1+\beta}$

2)Relation between α and γ :-

As , $\gamma = \frac{\Delta I_E}{\Delta I_B} = \frac{\Delta I_E}{\Delta I_E - \Delta I_c} = \frac{\Delta I_E/\Delta I_E}{1-\Delta I_C/\Delta I_E} = \frac{1}{1-\alpha}$

As , $\alpha = \frac{\Delta I_C}{\Delta I_E} = \frac{\Delta I_E - \Delta I_B}{\Delta I_E} = \frac{\Delta I_E/\Delta I_B - 1}{\Delta I_E/\Delta I_B} = \frac{\gamma - 1}{\gamma}$

3)Relation between β and γ :-

$$\text{As}, \quad \gamma = \frac{\Delta I_E}{\Delta I_B} = \frac{\Delta I_B + \Delta I_C}{\Delta I_B} = \frac{\Delta I_B}{\Delta I_B} + \frac{\Delta I_C}{\Delta I_B} = 1 + \beta$$

$$\text{As}, \quad \beta = \frac{\Delta I_C}{\Delta I_B} = \frac{\Delta I_E - \Delta I_B}{\Delta I_B} = \frac{\Delta I_E}{\Delta I_B} - \frac{\Delta I_B}{\Delta I_B} = \gamma - 1$$

4)Relation between α ,β and γ :-

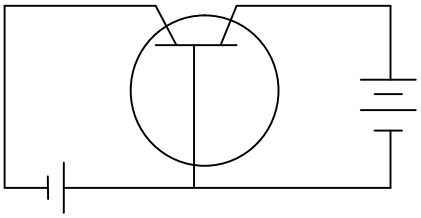
$$\text{As}, \quad \beta = \frac{\alpha}{1-\alpha} = \alpha \times \frac{1}{1-\alpha} = \alpha \times \gamma$$

$$\therefore \beta = \alpha \times \gamma$$

7marks questions

Q.State different configuration of transistor with neat circuit diagram [2014].

1)common base configuration –



In this type of configuration ,input is connected between base emitter and output is connected between base and collector .

So , in common base input is at emitter and output is at collector .

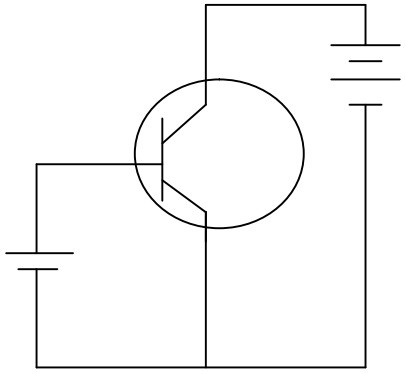
Here , I_E=input current

I_C=output current

V_{BE}=input voltage

V_{CB}=output voltage

2)common emitter configuration –



In common emitter configuration ,input is given at base w.r.t. emitter and output is collected at collector w.r.t. emitter .So , emitter is common to input aswell as to the output .

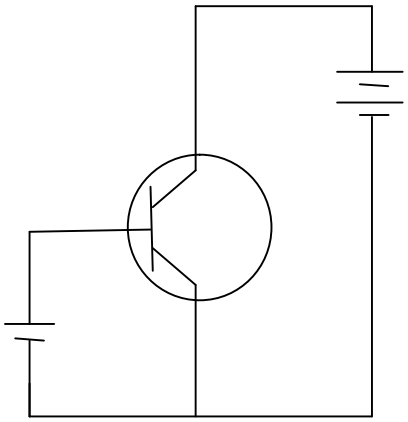
Here , I_B= input current

I_C=output current

V_{BE}=input voltage

V_{CE}=output voltage

3)common collector configuration :-



Here collector is common to both input and output circuit .

Here , I_B= input current

I_E=output current

V_{BC}=input voltage

V_{CE}=output voltage

Chapter -5

2 marks qustions

Q.What is the need of biasing [2014].

Linear circuit involving transistors typically require specific DC volage and currents for correct operation ,which can be achieved by using a biasing circuit .Basically the bias on a transistor is used to set the operating point of the transistor

Q.Define stabilisation [2015].

The process of making operating point independent of temperature charges or variations in transistor parameters is known as stabilisation .

Need for stabilisation :-

Stabilisation of the operating point is necessary du to the following reasons .

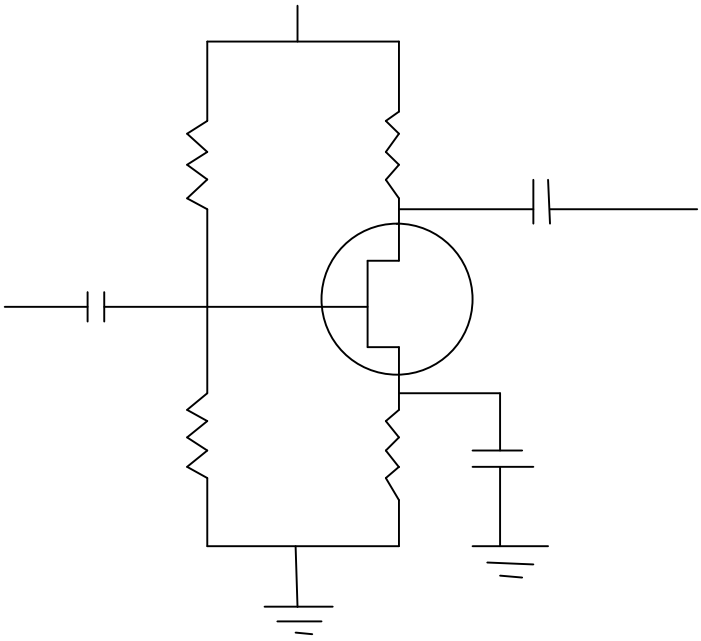
1.temperature dependence of I_C .

2.individual variations

3.thermal runaway

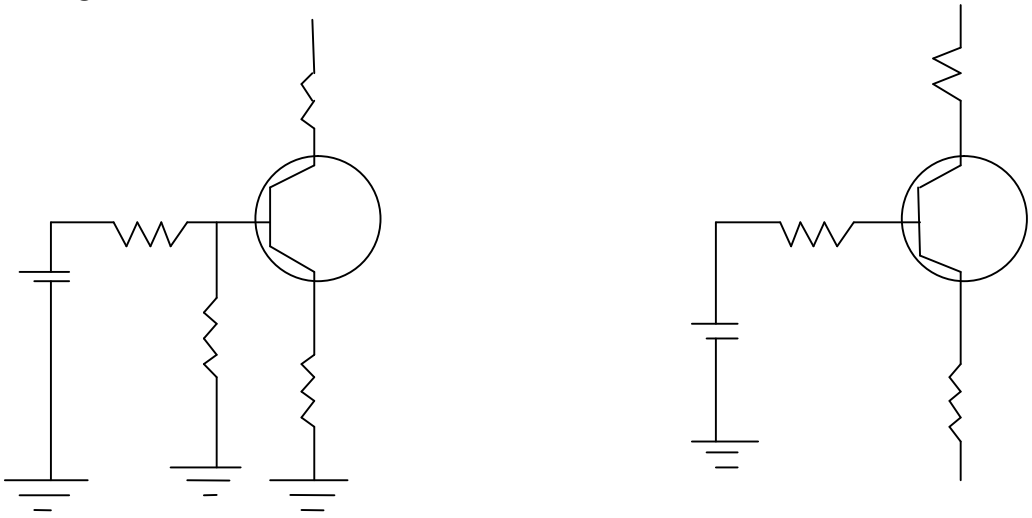
5 marks questions

Q.Explain voltage divider biasing with a neat circuit diagram in terms of stability factor [2015] .



The capacitors c_i ,c_o and c_s are open circuited in biasing analysis.It is called voltage divider biasing because the voltage appeared across R_2 is the voltage to the input of circuit .

Thebiasing circuit becomes :



V_{DS}

$V_{Th} = \frac{R_2 V_{DD}}{R_1 + R_2}$

$R_{Th} = R_1 \parallel R_2$

By input kvl

$$V_{Th} - V_{GS} - I_D R_S = 0$$

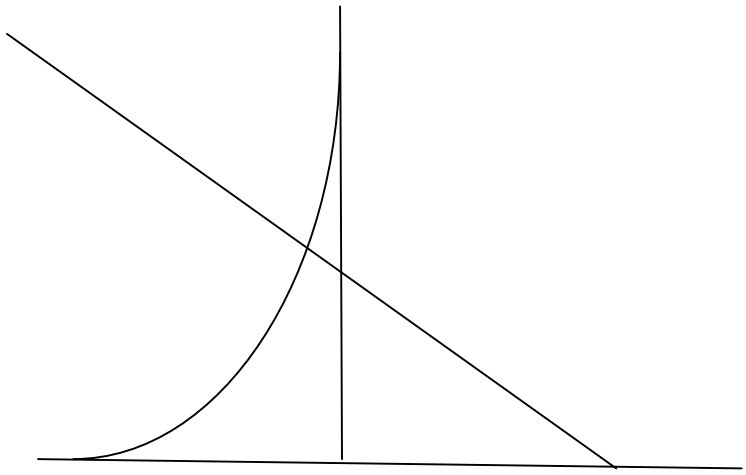
$$V_{GS} = V_{Th} - I_D R_S$$

Transfer line equation

V_{GS}	I_D
V_{Th}	0
0	V_{Th}/R_s

The transfer characteristic graph is plotted by the table

$V_{GS}(v)$	$I_D(mA)$
0	I_{DSS}
0.3 V_P	$I_{DSS}/2$
0.5V_P	$I_{DSS}/4$
V_P	0



From intersection point ,I_{DQ} & V_{GSQ} are determined

By output KVL

$\mathrm{V}_{\boldsymbol{DD}} - \mathrm{I}_{\boldsymbol{D}} R_{\mathbf{D}} - \mathrm{V}_{\boldsymbol{DS}} - I_D R_S = 0$

$$V_{DS} = V_{DD} - I_D(R_D + R_S)$$

Stability factor

Stability factor ,S= $\frac{(\beta+1)(R_D+R_E)}{R_0+R_E+\beta R_E}$

$$= (\beta + 1) \times \frac{1 + \frac{R_D}{R_E}}{\beta + 1 + \frac{R_D}{R_E}}$$

Where ,$R_0 = \frac{R_1 R_2}{R_1+R_2}$

If the ratio R_0 /R_E is very small ,then it is neglected as compared o 1 and the stability factor becomes $= (\beta + 1) \times \frac{1}{\beta+1} = 1$

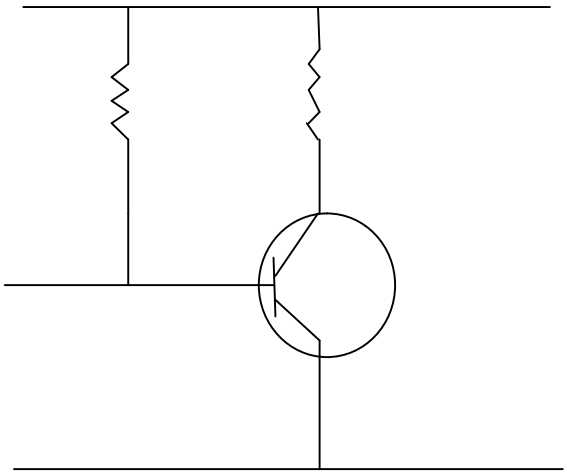
7 markes questions

Q.Define stability factor ,explain the base resister method of transister biasing [2014].

Base resister method :-

In this method ,a high resistance R_B is connected between the base and +ve end of supply for npn transistor and between base and –ve end of supply for pnp transistor .Here the required zero signal base current is provided by vcc and it flows through R_B .It is because now base is +ve w.r.t. emitter i.e base emitter junction is forward biased .The required value of zero signal base current I_B can be made to flow by selecting the proper value of base register R_B .

Circuit analysis :-



$$I_B = \frac{I_C}{\beta}$$

$$V_{CC} = I_B R_B + V_{BE}$$

$$I_B R_B = V_{CC} - V_{BE}$$

$$R_B = \frac{V_{CC} - V_{BE}}{I_B}$$

V_{BE} is small so ng;ected

$$R_B = \frac{V_{CC}}{I_B}$$

Stability factor

$$s = \frac{\beta + 1}{1 - \beta(\frac{dI_B}{dI_C})}$$

Here I_B is independent of I_C .so that $dI_B/dI_C = 0$

Putting the value of this in the above expression ,we have .s=β+1

Chapter 6

2 markes questions

Q.Write the types of oscillator [2014]

A device for generating oscillatory electronic currents or voltage by non mechanical means .

There ase different types of oscillators ,they are

- Tuned colletor oscillator
- Colpitt's oscillator
- Hartley oscillator
- Phase shift oscillator
- Wein bridge oscillator
- Crystal oscillator

Q.Define oscillator ?[2015]

An oscillator is a mechanical or electronic device that works on the principles of oscillation :a periodic fluctuation between two things based on changes in energy .

Computer ,clocks ,watches ,radios and metal detectors are among the many devices that use oscillators .

5 marks question

Q.Explain the essentials of transistors oscillator [2014] .

Its essential components are :

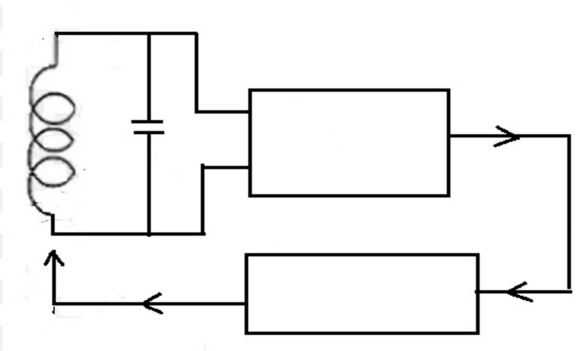
- Tank circuit

It consists of inductance coil connected in parallel with capacitor .the frequency of oscillation in the circuit depends upon the values of inductance of the coil and capacitance of the capacitor .

- Transistor amplifier

The transistor amplifier receives d.c. power from the battery and changes it into a.c. power for supplying to the tank circuit .The oscillations occurring in the tank circuit are applied to the input of the transistor amplifier .

Because of the amplifying properties of the transistor , we get increased output of these oscillations .



This amplified output of oscillation is due to the d.c. power supplied by the battery .The output of the transistor can be supplied to the tank circuit to meet the losses .

- Feedback circuit

The feedback circuit supplies a part of collector energy to the tank circuit in correct phase to aid the oscillations ,it provides positive feedback .

Q.<u>Explain the principle of operation of Hartley oscillator with a neat diagram [2014] .</u>

Hartley oscillator :

The Hartley oscillator is similar to colpitt's oscillator with minor modifications .instead of using tapped capacitors ,two inductors L_1 and L_2 are

place across a common capacitor C and the center of the inductors is tapped as shown in figure .The tank circuit is made up of L_1 ,L_2 and C .The frequency of oscillations is determined by the values of L_1 ,L_2 and C is given by :

$$F = \frac{1}{2\pi\sqrt{CL_T}}$$

$$L_T = L_1 + L_2 + 2M$$

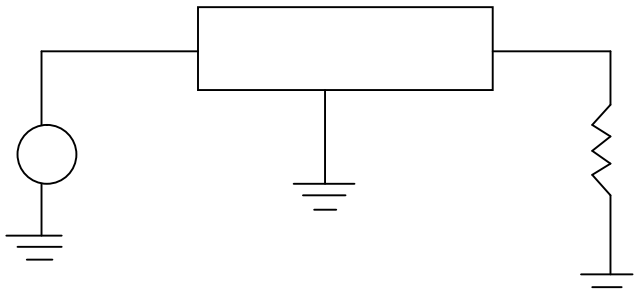
M= mutual inductance between L_1 and L_2

Circuit operation :

When the circuit is turned on ,the capacitor is charged .When this capacitor is fully charged ,it discharges through coils L_1 and L_2 setting up oscillations of frequency determined by the output voltage of the amplifier appears across L_1 and feedback voltage across L_2 .The voltage across L_2 is 180° out of phase with the voltage developed across L_1 .It is easy to see that voltage feedback to the transmitor provides +ve feedback .A phase shift of 180° is produced by the transistor and a further phase shift of 180° is produced by $L_1 – L_2$ voltage divider in this way feedback is properly phased to produced continuous undamped oscillation .

Q.Define transistors in terms of hybrid parameters

When linear circuit is terminated by load r_L ,we can find input impedance ,current gain ,voltage gain etc .In terms of h parameters fortunately ,for small a.c. signals ,the transistor behaves as a linear device because the output a.c. signal is directly proportional to the input a.c. signal .Under such circumstances ,the a.c. operation of the transistor can be described in terms of h parameters .The expressions derived for input impedance ,voltage gain etc .



There are 4 quantities required to describe the external behavior of the transistor amplifier .These are V_1 ,i_1 ,V_2 and i_2 shown on the diagram .These voltages and currents can be related by the following sets of equations :

$$v_1 = h_{11}i_1 + h_{12}v_2$$

$$i_2 = h_{21}i_1 + h_{22}v_2$$

The following points are worth nothing while considering the behavior of transistor in terms of h parameters .

1. For small a.c. signal ,a transistor behaves as a linear circuit .Therefore ,it's a.c. operation can be decribed in terms of h parameters .

2.The value of h parameters of a transistor will depend upon the transistor connection used .For instance ,a transistor used in CB arrangement may have h_{11}=20Ω .If we use the same transistor in CE arrangement , h_{11} will have a differentvalue .Same is the case will other h parameters .

3.The parameters for input impedance ,voltage gain etc .It also applicable to transistor amplifier except that r_L is the a.c. load seen by the transistor i.e

$$r_{L=R_C \| R_L}$$

4.The values of h parameters depend upon the operating point .If the operating point is changed ,parameter values are also changed .

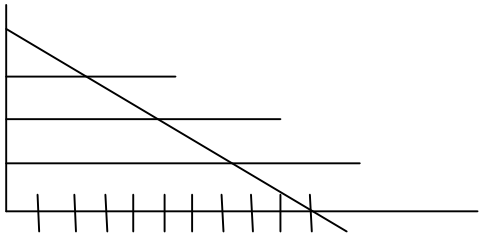
5.The notation V_1, i_1,V_2 and i_2 are used for general circuit analysis In a transistor amplifier we use the notation depending upon the configuration in which transistor is used .Thus for CE arrangement

$$V_1 = V_{be}\ ; i_1 = I_b\ ; V_2 = V_{ce}\ , i_2 = I_c$$

Here $V_{be}\ , I_b\ , V_{ce}\ and\ I_c$ are the R.M.S. values.

Q. Explain DC load line analysis of CE configuration of a transistor [2015] :

The below figure show the output characteristic curves for the transistor in CE mode .The DC load line is drawn on the output characteristic curves



Load line :

To draw load line ,we have to find saturation current and the cutoff voltage .After plotting these values on the vertical and the horizontal axis ,a line is drawn joining these two points ,which represents DC load line ‘

It represents all possible combinations of the collector current I_c and the collector voltage V_c for the given load registor RC .

Q.Explain principal operation of a wein bridge oscillator [2015].

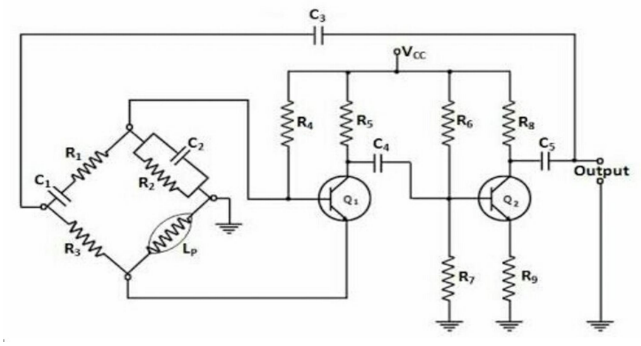
The wein bridge oscillator is the standard oscillator circuit for all frequencies in the range of 10HZ to about 1MH_z .It is the most frequently used type of audio oscillator as the output is free from circuit fluctuations and ambient temp .

It is essentially a 2 stage amplifier with R-C bridge circuit .The bridge circuit has the arms R_1C_1 ,R_3 ,R_2C_2 and tungsten lamp L_p .Resistances R_3 and L_p are

used to stabilize the amplitude of the output .The transistor T_1 serves as an oscillator and amplifier while the other transistor T_2 serves as an inverter .The circuit uses +ve and –ve feedbacks .The +ve feedback is through R_1C_1 ,R_2C_2 to the transistor T_1 .The –ve feedback is through the voltage divider to the input of transistor T_2 .The frequency of oscillations is determined by the series element R_1C_1 and parallel element R_2C_2 of the bridge .

$$f = \frac{1}{2\pi\sqrt{R_1C_1R_2C_2}}$$

If $R_1=R_2=R$ and $C_1=C_2=C$ then $f=\frac{1}{2\pi R_C}$

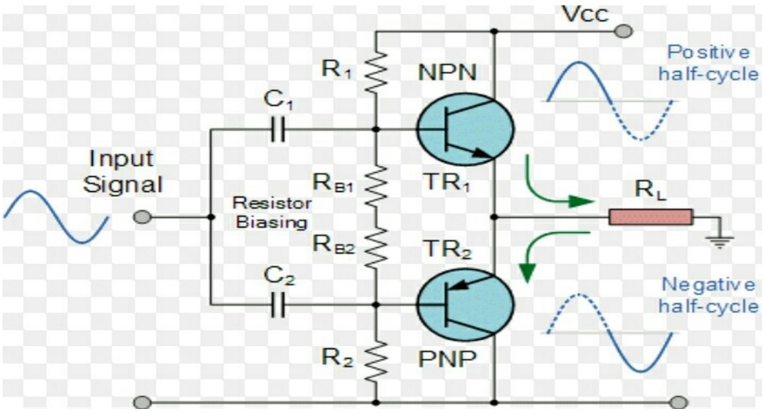


7 markes questions

Q.Explain the principle of operation of class B push-pull amplifier with a neat diagram [2014] .

When a transistor in operated as class B ,it clips off half the cycle .In order to avoid distortion we use 2 transistors in push-pull arrangement .Durring the -ve cycle the upper transistor turns off and lower one turns on .Since transistor amplifies half of input ,loud speaker receives a full cycle of the amplified signal .

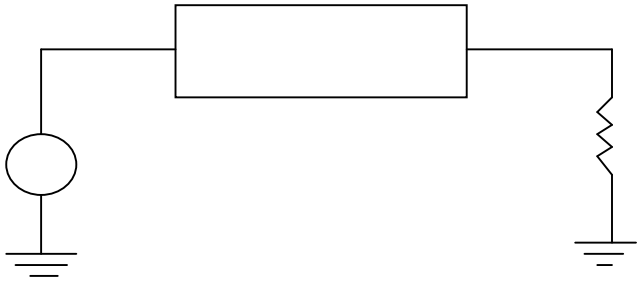
In order to improve the full power efficiency of the previous class A amplifier by reducing the wasted power in the form of heat .It is possible to design the power amplifier circuit with two transistors in its output stage producing what is commonly termed as a class B amplifier also known as push-pull amplifier configuration



Q.H parameters of transistor [2014] .

It has been in the previous seletion that every linear circuit is associated with h parameters .When this linear circuit is terminated by load r_L ,we can find input impedance ,current gain ,voltage gain etc .In terms of h parameters .

Fortunately ,for small a.c. signals ,the transistor behaves as a linear device because the output a.c. signal is directly proportional to the input a.c. signal .Under such circumstances ,the a.c. operaton of the transistor can be described in terms of h parameters .The expressions derived for input impedance ,voltage gain etc .In the previous section shall hold good for transistor amplifier except that here r_L is the a.c. load seen by the transistor .



Here the transistor amplifier circuit .There are 4 quantities required to describe the external behavior of the transistor amplifier .These are $V_1, i_1, V_2 \; and \; i_2$ shown on the diagram .These voltages and current can be related by the following sets of equations :

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The following points are worth nothing while considering the behavior of transistor in terms of h parameters :

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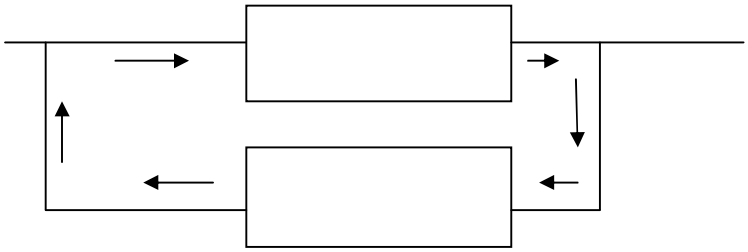
3.The expressions for input impedance ,voltage gain etc .

4.The value of h parameters depend upon the operating point .If the operating point is changed ,parameters values are also changed .

Q.<u>Negative feedback circuit [2014].</u>

When the feedback energy is out of phase with the input signal and thus opposes it ,it is called negative feeback .This is illustrated in this figure .As you can see ,the amplifier introduces a phase shift of 180° into the circuit while the feedback network is so dsigned that it introduces no phase shift .The result is that the feedback voltage V_f is 180° out of phase with the input signal V_{in}



Negative feedback reduces the gain of the amplifier .However ,the advantages of negative feedback are : reduction ,stability in gain ,increased bandwidth and improved input and output impedances .It is due to these advantages that –ve feedback is frequently employed in amplifier .

Gain stability :

An important advantage of negative voltage feedback is that the resultant gain of the amplifier can be made independent of transistor parameters of the supply voltage variations .

$$A_{vf} = \frac{A_v}{1 + A_v m_v}$$

Reduced non-linear distortion :

A large signal stage has non –linear distortion which is reduced by a factor (1+Aβ) when –ve feedback is used .

Reduced Noise :

There is always a noise voltage in the amplifier which is reduced by a factor (1+Aβ) when negative feedback is used .

Increased input impedance :

The input impedance of the amplifier with negative feedback is increased by a factor (1+Aβ) .

Q.Describe the working of class A push pull amplifier [2015] .

A push pull amplifier can be made in class A ,class B ,class AB or class C configurations .The circuit diagram of a typical class A push pull amplifier is

shown above .Q_1 and Q_2 are two identical transistor and their emitter terminals are connected together .R_1 and R_2 are meant for biasing transistors .Collector terminals of the two transistor are connected to the respective ends of the primary of the output transformer T_2 .Power supply is connected between the center tap of the T_2 primary and the emitter junction of the Q_1 and Q_2 .Base terminal of each transistor is connected to the respective ends of the second of the input coupling transformer T_1 .Input signal is applied to the primary of T_1 and output load R_L is connected across the secondary of T_2 Quiescent current of Q_2 and Q_1 flows in opposite directions through the corresponding halves of the primary of T_2 and as a result there will be no magnetic saturation .

From the figure we can see the phase splited signals being applied to the base of each transistors .When Q_1 is driven +ve using the first half of its input signal ,the collector current of Q_1 increases .At the same time Q_2 is driven –ve using the 1st half of its signal and so the collector current of Q_2 ,decreases .From the figure you can understand that the collector currents of Q_1 and Q_2 i.e 11 and 12 flows in the same direction through the corresponding halves of the T_2 primary .As a result an amplified version of the original input signal is induced in the T_2 secondary .It is clear that the current through the T_2 secondary is the difference between the 2 collector currents .

Chapter 7

7 markes questions

Q.Describe the different biasing of FET [2014] .

JFET :

1 .Fixed biasing :

$$V_{DD} - I_D R_D - V_{DS} = 0$$

$$V_{DS} = V_{DD} - I_D R_D$$

here $V_s = 0$

$$V_D = V_{DS} + V_S = V_{DD} - I_D R_D$$

$$V_G = V_{GS} + V_S = -V_{GG}$$

2 .Self stabilized biasing :

$$V_{DD} - I_D R_D - V_{DS} - I_D R_S = 0$$

$$V_{DS} = V_{DD} - I_D(R_D + R_S)$$

Here $V_s = I_D R_S$

$$V_G = 0$$

$$V_D = V_{DS} + V_S = V_{DD} - I_D R_D$$

3.Voltage divider biasing :

Type equation here.

$$V_{DD} - I_D R_D - V_{DS} - I_D R_S = 0$$

$$V_{DS} = V_{DD} - I_D(R_D + R_S)$$

Here $V_S = I_D R_S$

$$V_G = V_{GS} + V_S \; or V_G = V_{Th} - I_G R_S = V_{Th}$$

$$V_D = V_{DS} + V_S = V_{DD} - I_D R_D$$

MOSFET :

This is a type of FET ,where gate is made up sio_2 layer and metal is used to have contacts .So it is named as metal oxide semi conductor FET (MOSFET) .

In mosfet there are 4 terminals :

Source ,Gate ,Drain ,Substrate

Q.<u>State advantages of FET over BJT</u> .

FET	BJT
Voltage controlled current source sourse	Current controlled current
Unipolar device	Bipolar device
Require less construction area required	Relatively layer area is
High input impedance	Low input impedance
There is no offset voltage problem	It suffers from offset voltage
Early effect and thermal run away	Early effect and thermal run away
Problems are not observed .	problems are present .
Less noisy .	more noisy
Less sensitive to the charge in input Signal .	High sensitive to charge in input signal .
More temperature stability .	Less temperature stability .
Low power rating ,	High power rating .

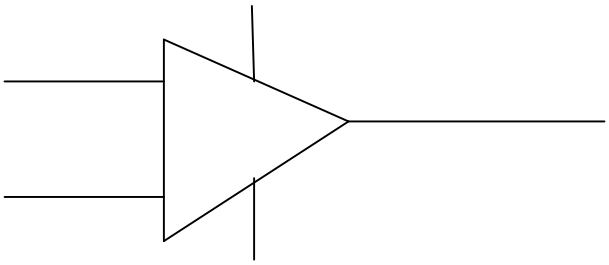
Chapter 8

<u>2 markes questions</u>

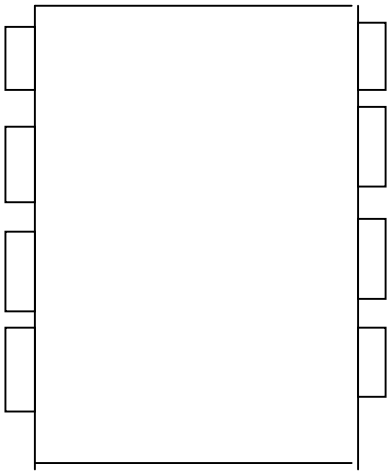
Q.<u>What is OP-Amp ?[2014] .</u>

An operational amplifier is a DC coupled high gain electronic voltage amplifier wih a differential input and usually a single ended output .

It is of discrete and integrated type .1st produce in 1941 .



Q.<u>Draw the pin diagram for 741 IC OP-AMP ?[2015]</u>

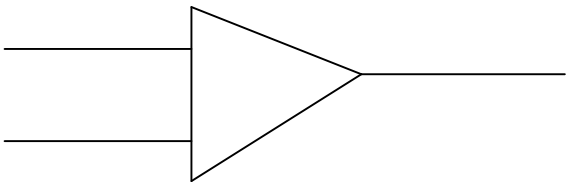


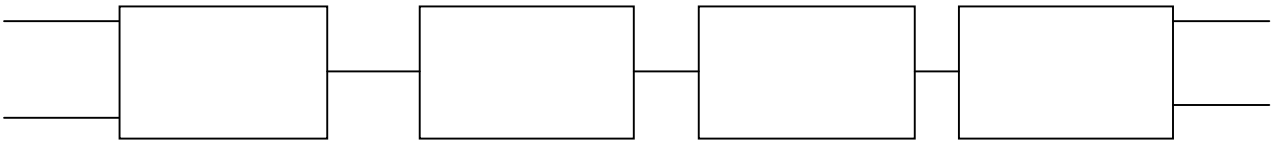
5 markes questions

Q.Describe the stages of operational amplifier [2014] .

The operational amplifier of op-amp is a direct coupled , high gain amplifier used to perform a wide variety of mathematical operation like summation ,substration ,multiplication ,differentation and integration etc .

The symbol and the block diagram of an operational amplifier are shown below .





Differential amplifier :-

The differential amplifier provides ,the inverting and non inverting inputs ,the high common mode rejection ratio and the high input resistance as well as voltage gain .

Gain stage :-

The interior stage of the op-amp is required to have a large voltage gain .

Level shifter :-

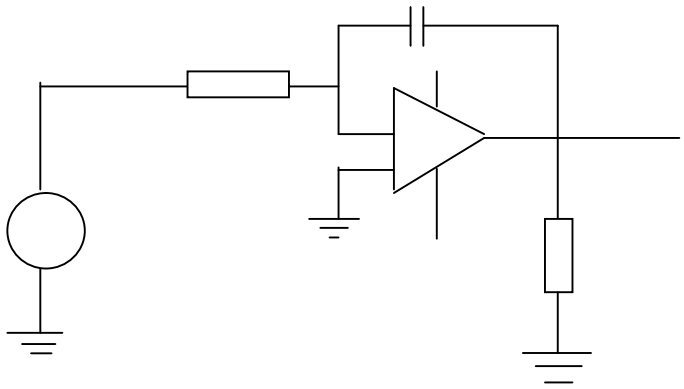
Since no coupling capacitors can be used .It may be necessary to shift the quiescent voltage of one stage before applying itsoutput to the folowing stage .Lebel shifting is also required in order for the output to be close to zero in the quiescent state .

Output state :-

The output stage of an op-amp must be capable of supplying the external load current and must have a low output resistance .This stage must also provide a large output voltage swing .

Q.<u>Construct and explain the working of an integrator using Op-Amp [2015] .</u>

The operational amplifier integrator is an electronic integration circuit .Based on the operational amplifier (Op-Amp) , it performs the mathematical operation of integration w.r.t. time ;that is the output voltage is propertional to the input voltage integrated over time .



If the op-amp is assumed to be ideal ,nodes V_1 and V_2 are held equal and so V_2 is a virtual ground .The input voltage passes a current $\frac{V_{in}}{R_1}$ through the resisteor .

The circuit can be analyzed by applying kirchhoff's current law at the node V_2

$$i_1 = I_B + i_F$$

$$I_B = 0$$

$$i_1 = i_F$$

$$I_c = C\frac{dv_c}{dt}$$

$$\frac{V_{in} - V_2}{R_1} = C_F\frac{(V_2 - V_0)}{dt}$$

$$V_2 = V_1 = 0$$

So ,$\frac{V_{in}}{R_1} = -C_F \frac{dV_0}{dt}$

Integrating both sides ,

$$\int_0^t \frac{V_{in}}{R_1} dt = -\int_0^t C_F \frac{dV_0}{dt} dt$$

In the initial value of V_0 isassumed to be 0v ,this results in a Dc error of

$$V_0 = -\frac{1}{R_1 C_F} \int_0^t V_{in} dt$$